Docket No. A5GN2102US PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:	:	Group Art Unit: 2611
Applicants: Rodney Dean Miller	:	
Filed: November 18, 2003	:	Examiner: Ha, Dac V
Serial No. 10/717,394	:	
For: PHASE-LOCKED LOOP STRUCTURES WITH ENHANCED SIGNAL STABILITY	:	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF RODNEY DEAN MILLER

I, Rodney Dean Miller, declare:

1. I am one of the inventors of the invention which is the subject of the above-identified patent application.

2. At all times mentioned herein I was a Design Engineer for Analog Devices, Inc., the assignee of the present invention, and I am presently a Senior Design Engineer for Analog Devices, Inc.

3. Attached as Exhibit 1 is a schematic of a phase-locked loop (marked PLL) that is dated March 6, 2000 in the lower left corner and has a part number 9887 and another description of "phase lock generator" in the upper left corner (although the phase lock generator has many applications, one exemplary use is in the AD9887 which is an analog and digital interface for flat panel displays – thus the part number 9887). This schematic shows, at its right side, a voltage-controlled oscillator (marked VCO) which provides 12 output signals (at extreme right side marked CPH0-CPH11) which have the same VCO frequency but which provide 6 different VCO phases (and 6 additional phases that are 180 degrees from the initial 6 phases).

At lower center, the PLL schematic shows a loop frequency divider (marked clkgen) that receives (at two ports CPH5 and CPH6) one of the six VCO output signals (and its inversion) and provides a divided feedback signal (marked FDBCLK) to a phase detector at the center left which receives a second input signal from an input flip-flop (marked L). This flip-flop is arranged to divide an input signal marked REFCLK which is the PLL input signal (the upper of three input signals at left side). The flip-flop thus provides to the phase detector a loop input signal whose frequency is one half that of REFCLK.

The output of the phase detector goes to a phase pump (marked cpmp) and the control voltage out of the phase pump goes through a loop filter (first capacitor in parallel with a series combination of a resistor and a second capacitor). The filtered control voltage is fed to the VCO to control the frequency of the VCO output signals.

A controller is shown at the lower right of the PLL schematic. Details of this controller are described below in Exhibit 4 but, basically, the controller also receives the filtered control voltage from the charge pump and, in response, generates three output signals marked Aout, Bout and Cout which go to each inverter stage in the VCO (in Exhibit 1 they are directed off to the lower right).

When the controller senses that the control voltage moves out one side of a predetermined control-voltage range, it generates Aout and when it senses that the control voltage moves out the other side of the predetermined control-voltage range, it generates Cout. The controller is also configured to sense when the control voltage is in the middle of a new control-voltage range and, in response, it generates Bout. These signals are processed through other circuits (not shown) for other purposes and are brought back in through multiplexers (at top right) and enter the VCO as signals Q0 and Q1. In Exhibit 4 (which will be described below), each control-voltage range is called a "gear" so that Exhibit 4 is entitled "Gear Control" rather than simply "Controller". The control-voltage ranges (or gears) are shown as tuning curves 43-48 and103-108 in FIGS. 2 and 6 of the application.

The VCO of Exhibit 1 is the VCO in FIGS. 1 and 3 of the application and the oscillator of independent claims 1 and 7. The oscillator loop frequency divider, the phase comparator, the charge pump and the loop filter of Exhibit 1 form a feedback loop that generates the control voltage of the VCO as shown in FIGS. 1 and 3 of the application and recited in independent claims 1 and 7. In addition, the controller of Exhibit 1 senses when the control voltage moves out of a predetermined control-voltage range and generates signals (Aout and Cout) to increment a frequency-determining parameter of the VCO as shown in FIGS. 1 and 3 of the application and recited in claims 1 and 7.

4. Attached as Exhibit 2 is a schematic of an embodiment of the VCO of Exhibit 1. This schematic is dated March 22, 2002 (in the title block in lower right) and shows six inverters (upper part of schematic) that are coupled in a ring. An output signal from each of the inverters goes upwards through a respective one of six buffers to thereby provide the 12 phase-shifted VCO output signals (CPH0-CPH11) that were described above with reference to Exhibit 1. At the lower left is circuitry which collectively forms the V-I converter (voltage-to-current converter) 83 in FIGS. 5A-5C of the application. This V-I converter is completed by tail current transistors to thereby convert the control voltage (from the charge pump of Exhibit 1) into a tail current as described in Exhibit 3 below.

The VCO if Exhibit 2 thus comprises a ring of inverters as shown in FIG. 4 of the application and recited in claims 9, 11, 13, 15 and 18.

5. Attached as Exhibit 3 is a schematic of each of the inverters (delay stages) of Exhibit 2. This schematic is dated February 16, 2001 (in the title block in lower right) and shows an embodiment in which each inverter comprises a differential pair (MP0, MP1) that steers a tail current from transistors MP2 and MP3 through resistive and capacitive loads. The load capacitors C52, C55 are coupled across the differential pair with switches that respond to signals Q1 and Q2 which were also shown entering the upper left of the VCO of Exhibit 1.

The drain ports Nout and Pout of the inverter stage of Exhibit 3 are coupled to the gate ports Nin and Pin of the succeeding one of these stages to thereby form the VCO ring of Exhibit 2.

The tail current transistors MP2 and MP3 form a final portion of the V-I converter circuitry in the lower left of Exhibit 2 which converts the control voltage (from the charge pump of Exhibit 1) into the tail current of the inverter stage in Exhibit 3.

The inverter of Exhibit 3 thus forms an inverter similar to those shown in FIGS. 5A and 5B of the application and recited in claims 11-14 which have resistive and capacitive loads.

The Aout and Cout signals from the controller in Exhibit 1 are conditioned (by circuitry not shown) into the signals Q1 and Q2 that switch in and out the load capacitors C52 and C55. Through various combinations of these load capacitors (e.g., none, one, the other, and both), an exemplary four of the tuning

curves (43-48 and103-108 in FIGS. 2 and 6 of the application) can be incremented to maintain the VCO control voltage within a predetermined control-voltage range as recited in independent claims 1 and 7.

6. Attached as Exhibit 4 is a schematic of the controller (called Gear Control) of Exhibit 1. This schematic is dated February 14, 2001 (in the title block in lower right) and shows a controller embodiment in which the filtered control voltage (PLLFLT) from the charge pump in Exhibit 1 is fed to three comparators which also receive reference voltages from a resistive ladder (arranged vertically at the left of the comparators). As the filtered control voltage crosses the reference voltages, the three comparators generate the signals Aout, Bout and Cout that are shown exiting buffers in the upper right. These are the same signals which were shown at the lower left in Exhibit 1 and initially described with respect to Exhibit 1.

At the middle left of Exhibit 4, a comparator takes an input from a resistive divider (R51, R52) and generates a mid-range control voltage that can be briefly applied through a control switch at the comparator output to the VCO in Exhibit 1. This mid-range control voltage is applied after a selected one of the signals Aout and Cout has been applied to increment the frequency-determining parameter of the VCO (to thereby move to an adjacent tuning range). The mid-range control voltage roughly centers the VCO on the new tuning curve. When the comparators sense and verify that the control voltage has settled at mid range, they generate the Bout signal of which then switches out the mid-range control voltage (with the control switch at the comparator output) so that the VCO is again controlled by the feedback loop.. This circuitry of Exhibit 4 thus briefly insures that the VCO is securely positioned on its new tuning curve after which it is switched out so that it does not impede subsequent loop operation.

The controller of Exhibit 4 is thus configured to monitor the VCO control voltage and select appropriate loads in the inverter of Exhibit 3 when the control voltage reaches one side of a control-voltage range as recited in claims 8, 10, 12, and 14.

7. Exhibits 1-4 thus disclose the oscillator (the VCO of Exhibit 2), the feedback loop (loop divider, phase comparator and charge pump of Exhibit 1), and the controller (shown in Exhibit 1 and detailed in Exhibit 4) that are recited in independent claims 1 and 7.

They also disclose how the controller of Exhibit 4 monitors the VCO control voltage and increments a frequency-determining VCO parameter each time the control voltage reaches a limit of the control-voltage range (as signaled by signals Aout and Cout in Exhibits 1 and 4) as particularly recited in claims 2, 5 and 8.

Exhibits 1-4 also disclose that the feedback loop comprises a phase detector, charge pump and loop filter as recited in claims 6 and 20.

Exhibits 1-4 also disclose the plurality of inverters recited in claims 9, 11, 13, 15 and 18 and discloses that inverter loads (such as those recited in claim 19) are selected each time the control voltage reaches a limit of a control-voltage range as signaled by signals Aout and Cout in Exhibits 1 and 4 and as recited in claims 12 and 14.

Exhibits 1-4 further disclose that each inverter comprises a voltage-to-current converter, a pair of loads and a differential pair of transistors as recited in claims 18 and 19.

8. Attached as Exhibit 5 is a 46-page layout verification and archive signoff that is dated February 14, 2002 and has a part number 9887A which links it to the part number 9887 in Exhibit 1. This layout verification and archive signoff confirms the readiness of the design for mask fabrication and archive as noted at the top of page 1. As noted at 3.0 of the first page, the layout has been checked with the schematic and, as noted at 5.0 of the second page, assembly guidelines have been followed during design and layout.

Foundry mask information is on page 3, chip dimensions are on page 4, pin layouts are on page 6, bond wire and bond pad specifications are on page 7, bond pad coordinates are on page 8, and page 9 lists hard drive locations (coded gremlin) for all files contained in the layout verification and archive signoff. The remaining pages of the layout verification and archive signoff contain all information for fabrication (e.g., capacitor lists on page 14, device types on page 16, transistor lists on page 35, and number of devices on page 43).

9. Attached as Exhibit 6 is a 14-page test report that is directed to part type ad9887 (3rd line on page 1), is based on 1125 tests of 388 devices (16th line on page 1), and is dated March 21, 2003 (13th and 14th lines on page 1). The date of 1969 on the 15th line of page 1 is a known anomaly of the test setup which the test personnel have never bothered to clear from the test protocol. Of the 388 devices tested, the 4th column (marked "Fails") shows the number of devices that failed each of the 1125 tests and the 5th column shows the corresponding "Test Yield %".

As mentioned above, the PLL of Exhibits 1-4 can be used in numerous devices. One of these devices is an analog and digital interface for flat panel displays and the AD9887 of the test is such an interface. Only a subset of the 1125 tests, therefore, concerned the PLL of Exhibits 1-4. In this subset, the number of failed devices was 0 and the test yield percentage was 100%.

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: 4/2/07

Rodney Dean Miller